CLAIMS

1. A multiple die semiconductor assembly comprising:

a substrate;

a first semiconductor die including a pair of major surfaces, wherein

one of said pair of major surfaces of said first die defines a first active surface,

the other of said major surfaces of said first die defines a first stacking surface,

said first active surface includes at least one conductive bond pad, and

said first stacking surface is secured to said substrate; and

a second semiconductor die including a pair of major surfaces, wherein

one of said pair of major surfaces of said second die defines a second active surface,

the other of said major surfaces of said second die defines a second stacking surface,

said second active surface includes at least one conductive bond pad, and

said first semiconductor die is electrically coupled to said second semiconductor die by at least one topographic contact extending from a conductive bond pad on said second active surface to a conductive bond pad on said first active surface.

2. A multiple die semiconductor assembly comprising:

a substrate including a first surface and conductive contacts included on said first surface;

a first semiconductor die including a pair of major surfaces, wherein

one of said pair of major surfaces of said first die defines a first active surface,

the other of said major surfaces of said first die defines a first stacking surface,

said first active surface includes at least one conductive bond pad, and

said first stacking surface is secured to said first surface of said substrate;

a second semiconductor die including a pair of major surfaces, wherein

one of said pair of major surfaces of said second die defines a second active surface,

the other of said major surfaces of said second die defines a second stacking surface,

said second active surface includes at least one conductive bond pad,

said first semiconductor die is electrically coupled to said second semiconductor die by at least one topographic contact extending from a conductive bond pad on said second active surface to a conductive bond pad on said first active surface; and

at least one conductive line extending from a bond pad on said first active surface to a conductive contact on said first surface of said substrate.

3. A multiple die semiconductor assembly comprising:

a substrate including a first surface and conductive contacts included on said first surface;

a first semiconductor die including a pair of major surfaces, wherein

one of said pair of major surfaces of said first die defines a first active surface,

the other of said major surfaces of said first die defines a first stacking surface,

said first active surface includes at least one conductive bond pad, and

said first stacking surface is secured to said first surface of said substrate;

a second semiconductor die including a pair of major surfaces, wherein

one of said pair of major surfaces of said second die defines a second active surface,

the other of said major surfaces of said second die defines a second stacking surface,

said second active surface includes at least one conductive bond pad,

said first semiconductor die is electrically coupled to said second semiconductor die by at least one topographic contact extending from a conductive bond pad on said second active surface to a conductive bond pad on said first active surface;

at least one decoupling capacitor secured to said second stacking surface; and

at least one conductive line connecting said decoupling capacitor, a bond pad on said first active surface, and a conductive contact on said first surface of said substrate.

4. A multiple die semiconductor assembly comprising:

a substrate;

a first semiconductor die including a pair of major surfaces, wherein

one of said pair of major surfaces of said first die defines a first active surface,

the other of said major surfaces of said first die defines a first stacking surface,

said first active surface includes at least one conductive bond pad, and

said first active surface is electrically coupled to said substrate by at least one topographic contact extending from a conductive bond pad on said first active surface to a conductive contact on said substrate; and

a second semiconductor die including a pair of major surfaces, wherein

one of said pair of major surfaces of said second die defines a second active surface,

the other of said major surfaces of said second die defines a second stacking surface,

said second active surface includes at least one conductive bond pad, and

said first stacking surface is secured to said second stacking surface.

5. A multiple die semiconductor assembly comprising:

a substrate including a first surface and conductive contacts included on said first surface;

a first semiconductor die including a pair of major surfaces, wherein

one of said pair of major surfaces of said first die defines a first active surface,

the other of said major surfaces of said first die defines a first stacking surface,

said first active surface includes at least one conductive bond pad, and

said first active surface is electrically coupled to said substrate by at least one topographic contact extending from a conductive bond pad on said first active surface to a conductive contact on said first surface of said substrate;

a second semiconductor die including a pair of major surfaces, wherein

one of said pair of major surfaces of said second die defines a second active surface,

the other of said major surfaces of said second die defines a second stacking surface,

said second active surface includes at least one conductive bond pad, and

said first stacking surface is secured to said second stacking surface; and

at least one conductive line extending from a bond pad on said second active surface to a conductive contact on said first surface of said substrate.

6. A multiple die semiconductor assembly comprising:

a substrate including a first surface and conductive contacts included on said first surface;

a first semiconductor die including a pair of major surfaces, wherein

one of said pair of major surfaces of said first die defines a first active surface,

the other of said major surfaces of said first die defines a first stacking surface,

said first active surface includes at least one conductive bond pad, and

said first active surface is electrically coupled to said substrate by at least one topographic contact extending from a conductive bond pad on said first active surface to a conductive contact on said first surface of said substrate;

a second semiconductor die including a pair of major surfaces, wherein

one of said pair of major surfaces of said second die defines a second active surface,

the other of said major surfaces of said second die defines a second stacking surface,

said second active surface includes at least one conductive bond pad, and

said first stacking surface is secured to said second stacking surface;

at least one decoupling capacitor secured to said second active surface; and

at least one conductive line connecting said decoupling capacitor, a bond pad on said second active surface, and a conductive contact on said first surface of said substrate.

7. A multiple die semiconductor assembly comprising:

a substrate;

a first semiconductor die defining a first active surface, said first active surface including at least one conductive bond pad;

a second semiconductor die defining a second active surface, said second active surface including at least one conductive bond pad, wherein said first semiconductor die is interposed between said substrate and said second semiconductor die such that a surface of said second semiconductor die defines an uppermost die surface of said multiple die semiconductor assembly and such that a surface of said first semiconductor die defines a lowermost die surface of said multiple die semiconductor assembly; and

at least one decoupling capacitor secured to said uppermost die surface and conductively coupled to at least one of said first and second semiconductor dies.

8. A multiple die semiconductor assembly defining a cross section, said assembly comprising:

a substrate;

a first semiconductor die positioned adjacent said substrate relative to said cross section;

a second semiconductor die positioned adjacent said first semiconductor die relative to said cross section, wherein said first semiconductor die is interposed between said substrate and said second semiconductor die relative to said cross section; and

at least one decoupling capacitor positioned adjacent said second semiconductor die relative to said cross section and secured to said second semiconductor die, wherein said second semiconductor die is interposed between said decoupling capacitor and said first semiconductor die relative to said cross section.

9. A printed circuit board assembly comprising:

a substrate;

a first semiconductor die including a pair of major surfaces, wherein

one of said pair of major surfaces of said first die defines a first active surface,

the other of said major surfaces of said first die defines a first stacking surface,

said first active surface includes at least one conductive bond pad, and

said first stacking surface is secured to said substrate;

a second semiconductor die including a pair of major surfaces, wherein

one of said pair of major surfaces of said second die defines a second active surface,

the other of said major surfaces of said second die defines a second stacking surface,

said second active surface includes at least one conductive bond pad, and

said first semiconductor die is electrically coupled to said second semiconductor die by at least one topographic contact extending from a conductive bond pad on said second active surface to a conductive bond pad on said first active surface;

a printed circuit board positioned such that a first surface of said printed circuit board faces said substrate; and

a plurality of topographic contacts extending from said substrate to said first surface of said printed circuit board.

10. A printed circuit board assembly comprising:

a substrate including a first surface and conductive contacts on said first surface;

a first semiconductor die including a pair of major surfaces, wherein

one of said pair of major surfaces of said first die defines a first active surface,

the other of said major surfaces of said first die defines a first stacking surface,

said first active surface includes at least one conductive bond pad, and

said first stacking surface is secured to said first surface of said substrate;

a second semiconductor die including a pair of major surfaces, wherein

one of said pair of major surfaces of said second die defines a second active surface,

the other of said major surfaces of said second die defines a second stacking surface,

said second active surface includes at least one conductive bond pad,

said first semiconductor die is electrically coupled to said second semiconductor die by at least one topographic contact extending from a conductive bond pad on said second active surface to a conductive bond pad on said first active surface;

at least one conductive line extending from a bond pad on said first active surface to a conductive contact on said first surface of said substrate;

a printed circuit board positioned such that a first surface of said printed circuit board faces said substrate; and

a plurality of topographic contacts extending from said substrate to said first surface of said printed circuit board.

11. A printed circuit board assembly comprising:

a substrate;

a first semiconductor die including a pair of major surfaces, wherein

one of said pair of major surfaces of said first die defines a first active surface,

the other of said major surfaces of said first die defines a first stacking surface,

said first active surface includes at least one conductive bond pad, and

said first active surface is electrically coupled to said substrate by at least one topographic contact extending from a conductive bond pad on said first active surface to a conductive contact on said substrate;

a second semiconductor die including a pair of major surfaces, wherein

one of said pair of major surfaces of said second die defines a second active surface,

the other of said major surfaces of said second die defines a second stacking surface,

said second active surface includes at least one conductive bond pad, and

said first stacking surface is secured to said second stacking surface;

a printed circuit board positioned such that a first surface of said printed circuit board faces said substrate; and

a plurality of topographic contacts extending from said substrate to said first surface of said printed circuit board.

12. A printed circuit board assembly comprising:

a substrate including a first surface and conductive contacts included on said first surface;

a first semiconductor die including a pair of major surfaces, wherein

one of said pair of major surfaces of said first die defines a first active surface,

the other of said major surfaces of said first die defines a first stacking surface,

said first active surface includes at least one conductive bond pad, and

said first active surface is electrically coupled to said substrate by at least one topographic contact extending from a conductive bond pad on said first active surface to a conductive contact on said first surface of said substrate;

a second semiconductor die including a pair of major surfaces, wherein

one of said pair of major surfaces of said second die defines a second active surface,

the other of said major surfaces of said second die defines a second stacking surface,

said second active surface includes at least one conductive bond pad, and

said first stacking surface is secured to said second stacking surface;

at least one conductive line extending from a bond pad on said second active surface to a conductive contact on said first surface of said substrate;

a printed circuit board positioned such that a first surface of said printed circuit board faces said substrate; and

a plurality of topographic contacts extending from said substrate to said first surface of said printed circuit board.

13. A printed circuit board assembly comprising:

a substrate;

a first semiconductor die defining a first active surface, said first active surface including at least one conductive bond pad;

a second semiconductor die defining a second active surface, said second active surface including at least one conductive bond pad, wherein said first semiconductor die is interposed between said substrate and said second semiconductor die such that a surface of said second semiconductor die defines an uppermost die surface of said multiple die semiconductor assembly and such that a surface of said first semiconductor die defines a lowermost die surface of said multiple die semiconductor assembly;

at least one decoupling capacitor secured to said uppermost die surface and conductively coupled to at least one of said first and second semiconductor dies;

a printed circuit board positioned such that a first surface of said printed circuit board faces said substrate; and

a plurality of topographic contacts extending from said substrate to said first surface of said printed circuit board.

14. A printed circuit board assembly comprising:

a substrate;

a first semiconductor die positioned adjacent said substrate relative to said cross section;

a second semiconductor die positioned adjacent said first semiconductor die relative to said cross section, wherein said first semiconductor die is interposed between said substrate and said second semiconductor die relative to said cross section;

at least one decoupling capacitor positioned adjacent said second semiconductor die relative to said cross section and secured to said second semiconductor die, wherein said second semiconductor die is interposed between said decoupling capacitor and said first semiconductor die relative to said cross section;

a printed circuit board positioned such that a first surface of said printed circuit board faces said substrate; and

a plurality of topographic contacts extending from said substrate to said first surface of said printed circuit board.

15. A printed circuit board assembly comprising:

a substrate including first and second surfaces and conductive contacts included on said first surface;

a first semiconductor die including a pair of major surfaces, wherein

one of said pair of major surfaces of said first die defines a first active surface,

the other of said major surfaces of said first die defines a first stacking surface,

said first active surface includes a plurality of conductive bond pads, and

said first stacking surface is devoid of conductive bond pads and is secured to said first surface of said substrate between said conductive contacts included on said first surface of said substrate;

a second semiconductor die including a pair of major surfaces, wherein

one of said pair of major surfaces of said second die defines a second active surface,

the other of said major surfaces of said second die defines a second stacking surface,

said second active surface includes a plurality of conductive bond pads,

said first semiconductor die is electrically coupled to said second semiconductor die by a plurality of topographic contacts extending from respective conductive bond pads on said second active surface to a corresponding conductive bond pad on said first active surface;

a single decoupling capacitor secured to said second stacking surface;

a pair of conductive lines, each of said conductive lines connecting a terminal of said decoupling capacitor, a bond pad on said first active surface, and a conductive contact on said first surface of said substrate, wherein said bond pad on said first active surface is electrically coupled to said second semiconductor die via one of said plurality of topographic contacts extending from respective conductive bond pads on said second active surface to a corresponding conductive bond pad on said first active surface, and wherein said pair of conductive lines are arranged such that said decoupling capacitor is connected across V_{ss} and V_{cc} pins of said first and second semiconductor dies;

a printed circuit board positioned such that a first surface of said printed circuit board faces said substrate; and

a plurality of topographic contacts extending from said second surface of said substrate to said first surface of said printed circuit board.

16. A printed circuit board assembly comprising:

a substrate including a first surface and conductive contacts included on said first surface;

a first semiconductor die including a pair of major surfaces, wherein

one of said pair of major surfaces of said first die defines a first active surface,

the other of said major surfaces of said first die defines a first stacking surface,

said first active surface includes a plurality of conductive bond pads, and

said first active surface is electrically coupled to said substrate by a plurality of topographic contacts extending from respective conductive bond pads on said first active surface to corresponding conductive contacts on said first surface of said substrate;

a second semiconductor die including a pair of major surfaces, wherein

one of said pair of major surfaces of said second die defines a second active surface,

the other of said major surfaces of said second die defines a second stacking surface,

said second active surface includes a plurality of conductive bond pads, and

said first stacking surface is devoid of conductive bond pads and is secured to said second stacking surface;

a single decoupling capacitor secured to said second active surface; and

a pair of conductive lines, each of said conductive lines connecting a terminal of said decoupling capacitor, a bond pad on said second active surface, and a conductive contact on said first surface of said substrate, wherein said conductive contact on said first surface of said substrate is electrically coupled to said first semiconductor die via one of said plurality of topographic contacts extending from respective conductive bond pads on said first active surface to corresponding conductive contacts on said first surface of said substrate, and wherein said pair of conductive lines are arranged such that said decoupling capacitor is connected across V_{ss} and V_{cc} pins of said first and second semiconductor dies;

a printed circuit board positioned such that a first surface of said printed circuit board faces said substrate; and

a plurality of topographic contacts extending from said substrate to said first surface of said printed circuit board.

17. A computer system comprising a programmable controller and at least one memory unit, wherein said memory unit comprises a printed circuit board assembly comprising:

a substrate;

a first semiconductor die including a pair of major surfaces, wherein

one of said pair of major surfaces of said first die defines a first active surface,

the other of said major surfaces of said first die defines a first stacking surface,

said first active surface includes at least one conductive bond pad, and

said first stacking surface is secured to said substrate;

a second semiconductor die including a pair of major surfaces, wherein

one of said pair of major surfaces of said second die defines a second active surface,

the other of said major surfaces of said second die defines a second stacking surface,

said second active surface includes at least one conductive bond pad, and

said first semiconductor die is electrically coupled to said second semiconductor die by at least one topographic contact extending from a conductive bond pad on said second active surface to a conductive bond pad on said first active surface;

a printed circuit board positioned such that a first surface of said printed circuit board faces said substrate; and

a plurality of topographic contacts extending from said substrate to said first surface of said printed circuit board.

18. A computer system comprising a programmable controller and at least one memory unit, wherein said memory unit comprises a printed circuit board assembly comprising:

a substrate;

a first semiconductor die including a pair of major surfaces, wherein

one of said pair of major surfaces of said first die defines a first active surface,

the other of said major surfaces of said first die defines a first stacking surface,

said first active surface includes at least one conductive bond pad, and

said first active surface is electrically coupled to said substrate by at least one topographic contact extending from a conductive bond pad on said first active surface to a conductive contact on said substrate;

a second semiconductor die including a pair of major surfaces, wherein

one of said pair of major surfaces of said second die defines a second active surface,

the other of said major surfaces of said second die defines a second stacking surface,

said second active surface includes at least one conductive bond pad, and

said first stacking surface is secured to said second stacking surface;

a printed circuit board positioned such that a first surface of said printed circuit board faces said substrate; and

a plurality of topographic contacts extending from said substrate to said first surface of said printed circuit board.

19. A method of stacking a plurality of semiconductor die, said method comprising:

providing a substrate;

providing a first semiconductor die including a pair of major surfaces, wherein

one of said pair of major surfaces of said first die defines a first active surface,

the other of said major surfaces of said first die defines a first stacking surface, and

said first active surface includes at least one conductive bond pad;

securing said first stacking surface to said substrate;

providing a second semiconductor die including a pair of major surfaces, wherein

one of said pair of major surfaces of said second die defines a second active surface,

the other of said major surfaces of said second die defines a second stacking surface, and

said second active surface includes at least one conductive bond pad;

electrically coupling said first semiconductor die to said second semiconductor die with at least one topographic contact extending from a conductive bond pad on said second active surface to a conductive bond pad on said first active surface.

20. A method of stacking a plurality of semiconductor die, said method comprising:

providing a substrate;

providing a first semiconductor die including a pair of major surfaces, wherein

one of said pair of major surfaces of said first die defines a first active surface,

the other of said major surfaces of said first die defines a first stacking surface, and

said first active surface includes at least one conductive bond pad;

electrically coupling said first active surface to said substrate with at least one topographic contact extending from a conductive bond pad on said first active surface to a conductive contact on said substrate;

providing a second semiconductor die including a pair of major surfaces, wherein

one of said pair of major surfaces of said second die defines a second active surface,

the other of said major surfaces of said second die defines a second stacking surface, and

said second active surface includes at least one conductive bond pad; and

securing said first stacking surface to said second stacking surface.

21. A method of stacking a plurality of semiconductor die, said method comprising:

providing a substrate;

providing a first semiconductor die defining a first active surface, said first active surface including at least one conductive bond pad;

providing a second semiconductor die defining a second active surface, said second active surface including at least one conductive bond pad;

interposing said first semiconductor die between said substrate and said second semiconductor die such that a surface of said second semiconductor die defines an uppermost die surface of said multiple die semiconductor assembly and such that a surface of said first semiconductor die defines a lowermost die surface of said multiple die semiconductor assembly;

securing at least one decoupling capacitor to said uppermost die surface; and

conductively coupling said decoupling capacitor to at least one of said first and second semiconductor dies.

22. A method of stacking a plurality of semiconductor die along a cross section, said method comprising:

providing a substrate;

positioning a first semiconductor die adjacent said substrate relative to said cross section;

positioning a second semiconductor die adjacent said first semiconductor die relative to said cross section;

interposing said first semiconductor die between said substrate and said second semiconductor die relative to said cross section;

positioning at least one decoupling capacitor adjacent said second semiconductor die relative to said cross section;

securing said decoupling capacitor to said second semiconductor die; and

interposing said second semiconductor die is between said decoupling capacitor and said first semiconductor die relative to said cross section.

23. A method of assembling a printed circuit board, said method comprising:

providing a substrate including first and second surfaces and conductive contacts included on said first surface;

providing a first semiconductor die including a pair of major surfaces, wherein

one of said pair of major surfaces of said first die defines a first active surface,

the other of said major surfaces of said first die defines a first stacking surface,

said first active surface includes a plurality of conductive bond pads, and

said first stacking surface is devoid of conductive bond pads;

securing said first stacking surface to said first surface of said substrate between said conductive contacts included on said first surface of said substrate;

providing a second semiconductor die including a pair of major surfaces, wherein

one of said pair of major surfaces of said second die defines a second active surface,

the other of said major surfaces of said second die defines a second stacking surface, and

said second active surface includes a plurality of conductive bond pads;

electrically coupling said first semiconductor die to said second semiconductor die with a plurality of topographic contacts extending from respective conductive bond pads on said second active surface to a corresponding conductive bond pad on said first active surface;

securing a single decoupling capacitor to said second stacking surface;

providing a pair of conductive lines, each of said conductive lines connecting a terminal of said decoupling capacitor, a bond pad on said first active surface, and a conductive contact on said first surface of said substrate;

electrically coupling said bond pad on said first active surface to said second semiconductor die via one of said plurality of topographic contacts extending from respective conductive bond pads on said second active surface to a corresponding conductive bond pad on said first active surface;

arranging said pair of conductive lines such that said decoupling capacitor is connected across V_{ss} and V_{cc} pins of said first and second semiconductor dies;

positioning a printed circuit board such that a first surface of said printed circuit board faces said substrate; and

providing a plurality of topographic contacts extending from said second surface of said substrate to said first surface of said printed circuit board.

24. A method of assembling a printed circuit board, said method comprising:

providing a substrate including a first surface and conductive contacts included on said first surface;

providing a first semiconductor die including a pair of major surfaces, wherein

one of said pair of major surfaces of said first die defines a first active surface,

the other of said major surfaces of said first die defines a first stacking surface, and

said first active surface includes a plurality of conductive bond pads;

electrically coupling said first active surface to said substrate with a plurality of topographic contacts extending from respective conductive bond pads on said first active surface to corresponding conductive contacts on said first surface of said substrate;

providing a second semiconductor die including a pair of major surfaces, wherein

one of said pair of major surfaces of said second die defines a second active surface,

the other of said major surfaces of said second die defines a second stacking surface,

said second active surface includes a plurality of conductive bond pads, and

said first stacking surface is devoid of conductive bond pads;

securing said first stacking surface to said second stacking surface;

securing a single decoupling capacitor to said second stacking surface;

providing a pair of conductive lines, each of said conductive lines connecting a terminal of said decoupling capacitor, a bond pad on said second active surface, and a conductive contact on said first surface of said substrate;

electrically coupling said conductive contact on said first surface of said substrate to said first semiconductor die via one of said plurality of topographic contacts extending from respective conductive bond pads on said first active surface to corresponding conductive contacts on said first surface of said substrate;

arranging said pair of conductive lines such that said decoupling capacitor is connected across V_{ss} and V_{cc} pins of said first and second semiconductor dies;

positioning a printed circuit board such that a first surface of said printed circuit board faces said substrate; and

providing a plurality of topographic contacts extending from said substrate to said first surface of said printed circuit board.

25. A multiple die semiconductor assembly as claimed in claim 1 wherein said first semiconductor die is secured to said substrate via a layer of die attach adhesive interposed between said substrate and said first semiconductor die.

26. A multiple die semiconductor assembly as claimed in claim 1 wherein said multiple die semiconductor assembly further comprises an encapsulant formed over at least a

portion of said first semiconductor die, at least a portion of said second semiconductor die, and at least a portion of said substrate.

27. A multiple die semiconductor assembly as claimed in claim 1 wherein said first semiconductor die is electrically coupled to said substrate.

28. A multiple die semiconductor assembly as claimed in claim 1 wherein said second semiconductor die is electrically coupled to said substrate.

29. A multiple die semiconductor assembly as claimed in claim 1 wherein said first semiconductor die and said second semiconductor die are electrically coupled to said substrate.

30. A multiple die semiconductor assembly as claimed in claim 3 wherein said bond pad on said first active surface is electrically coupled to said second semiconductor die.

31. A multiple die semiconductor assembly as claimed in claim 3 wherein said multiple die semiconductor assembly further comprises an encapsulant formed over at least a portion of said first semiconductor die, at least a portion of said second semiconductor die, at least a portion of said decoupling capacitor, and at least a portion of said substrate.

32. A multiple die semiconductor assembly as claimed in claim 4 wherein said multiple die semiconductor assembly further comprises an encapsulant formed over at least a portion of said second semiconductor die and at least a portion of said substrate.

33. A multiple die semiconductor assembly as claimed in claim 6 wherein said conductive contact on said first surface of said substrate is electrically coupled to said first semiconductor die.

34. A multiple die semiconductor assembly as claimed in claim 6 wherein said multiple die semiconductor assembly further comprises an encapsulant formed over at least a portion of said second semiconductor die, at least a portion of said decoupling capacitor, and at least a portion of said substrate.

35. A multiple die semiconductor assembly as claimed in claim 7 wherein said first and second active surfaces face each other.

36. A multiple die semiconductor assembly as claimed in claim 7 wherein said first and second active surfaces face away from each other.

37. A multiple die semiconductor assembly as claimed in claim 7 wherein said first die is secured to said substrate.

38. A multiple die semiconductor assembly as claimed in claim 7 wherein said first die is spaced from substrate by topographic contacts.

39. A multiple die semiconductor assembly as claimed in claim 8 wherein said first semiconductor die is spaced from said substrate by a plurality of topographic contacts.

40. A multiple die semiconductor assembly as claimed in claim 8 wherein said first semiconductor die is positioned directly adjacent said substrate within said cross section.

41. A multiple die semiconductor assembly as claimed in claim 40 wherein said first semiconductor die is secured to said substrate via a layer of die attach adhesive interposed between said substrate and said first semiconductor die.

42. A multiple die semiconductor assembly as claimed in claim 8 wherein said second semiconductor die is positioned directly adjacent said first semiconductor die within said cross section.

43. A multiple die semiconductor assembly as claimed in claim 42 wherein said second semiconductor die is secured to said first semiconductor die via a layer of die attach adhesive interposed between said first and second semiconductor dies.

44. A multiple die semiconductor assembly as claimed in claim 8 wherein said second semiconductor die is spaced from said first semiconductor die by a plurality of topographic contacts.